a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions; and

C6 cont.

interconnect structures contacting the semiconductor devices.

REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the following remarks.

The Applicant originally submitted Claims 1-33 in the application. In a previous response to an Official Action, the Applicant canceled Claim 33 without prejudice or disclaimer. Presently, the Applicant has amended Claims 1, 7, 12, 17, 21, and 27 and has neither canceled nor added any other claims. Accordingly, Claims 1-32 are currently pending in the application.

I. Rejection of Claims 1-32 under 35 U.S.C. §112

The Examiner has rejected Claims 1-32 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most clearly connected, to make and/or use the invention. The Examiner further states that each of the independent Claims requires an interface separating the first and second portions of the source/drain regions, and that the specification does not appear to provide enabling support for the claimed interface. First, the interface separating the

first and second portions of the source/drain regions is shown in FIGUREs 1, 11 and 12, and their supporting text. Second, as the material of the first and second portions of the source/drain regions was formed in separate steps, and not a single step as shown in the references, an interface must exist. Those skilled in the art of materials, easily understands this concept, and therefore, would have no problem making and/or using the presently claimed invention. Further, as the interface is only a material interface, the electrical contact between the first and second portions of the source/drain region is not impacted.

Further, the newly amended element of Claims 1, 7, 12, 17, 21 and 27 that no structural interface exists between the first and second portions of the isolation region, is not unclear as might be later suggested by the Examiner. For just the opposite reasons as mentioned above, this element is also clear. Namely, as the material for the first and second portions of the isolation region are formed in a single formation step, the material is continuous and no structural interface exists there between. In contrast, the material of the first and second portions of the prior art references were formed in multiple steps, and therefore an interface must exist.

As such, the Applicant requests that the Examiner kindly remove the §112 rejection with respect to Claims 1-32.

II. Rejection of Claims 1-5, 7-10, 12-14, 16, 17-19, and 21-25 under 35 U.S.C. §102

The Examiner has rejected Claims 1-5, 7-10, 12-14, 16, 17-19, and 21-25 under 35 U.S.C. §102(b) as being clearly anticipated by U.S. Patent No. 5,043,778 to Teng, et al. (Teng). Presently, newly amended independent Claims 1, 7, 12, 17, 21, and 27 include the element that no structural interface exists between the first and second portions of the isolation region. Teng fails to disclose

such an element, and actually teaches just the opposite. Because Teng teaches that its first isolation region portion (field oxide portion 20) is formed in a first step, and its second isolation region portion (dielectric 35) is formed in second subsequent step, an interface must exist between the two. For that reason, the interface is shown in Figs. 5a and 6 of the Teng reference. Accordingly, Teng fails to disclose the element that no structural interface exists between the first and second portions of the isolation region.

Therefore, Teng does not disclose each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, is not an anticipating reference. Because Claims 2-5, 8-10, 13-14, 16, 18-19, and 21-25 are dependent upon Claims 1, 7, 12, 17, 21 and 27, Teng also cannot be an anticipating reference for Claims 2-5, 8-10, 13-14, 16, 18-19, and 21-25. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to these Claims.

III. Rejection of Claims 6, 11, 15 and 26 under 35 U.S.C. §103

The Examiner has rejected Claims 6, 11, 15 and 26 under 35 U.S.C. §103(a) as being obvious over Teng in view of United States Patent Application No. 2002/0142552 A1 to Wu (Wu). As recited above, Teng fails to disclose every element recited in independent Claims 1, 7, 12, 17, 21 and 27. Namely, Teng fails to disclose the element that no structural interface exists between the first and second portions of the isolation region.

Similarly, it is the position of the Applicant that Teng also fails to suggest the element that no structural interface exists between the first and second portions of the isolation region. Teng fails to suggest such an element because Teng is focused on forming its first and second portions using multiple manufacturing steps. Given the structure illustrated and described in Teng, as well as the

method taught to manufacture such a device, one skilled in the art would not be motivated to manufacture the first and second portions having no structural interface located there between. That is, one skilled in the art would not be motivated to manufacture the first and second portions having no structural interface located there between because to do so would require forming the first and second portions in a single processing step, and such a step in not obvious in view of the teachings and suggestions of Teng. Accordingly, Teng also fails to teach or suggest such an element.

The Examiner is using the Wu reference for the sole proposition that the isolation region may extend through the transistor tub ("well"). Notwithstanding the merits of the Examiner's proposition, Wu also fails to teach or suggest the element that no structural interface exists between the first and second portions of the isolation region. A teaching or suggestion that the isolation region may extend through the transistor tub ("well") is dissimilar to a teaching or suggestion that no structural interface exists between the first and second portions of the isolation region.

Therefore, the combination of Teng and Wu fails to teach or suggest each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, it fails to establish a *prima facie* case of obviousness with respect to independent Claims 1, 7, 12, 17, 21 and 27, and any claims dependent therefrom.

In view of the foregoing amendments and remarks, the cited references do not support the Examiner's rejection of Claims 6, 11, 15 and 26 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

IV. Rejection of Claims 27-31 under 35 U.S.C. §103

The Examiner has rejected Claims 27-31 under 35 U.S.C. §103(a) as being obvious over Teng in view of the Applicant's admitted prior art (APA). As recited above, Teng fails to teach or suggest every element recited in independent Claims 1, 7, 12, 17, 21 and 27. Namely, Teng fails to teach or suggest the element that no structural interface exists between the first and second portions of the isolation region.

Similarly, the APA fails to teach or suggest such an element. The Examiner is using the APA for the sole proposition that interconnects may be used to connect the claimed device to various other active and passive devices. Notwithstanding the merits of the Examiner's proposition, the APA also fails to teach or suggest the element that no structural interface exists between the first and second portions of the isolation region. A teaching or suggestion of an interconnect connecting various devices is dissimilar to a teaching or suggestion that no structural interface exists between the first and second portions of the isolation region.

Therefore, the combination of Teng and the APA fails to teach or suggest each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, it fails to establish a *prima facie* case of obviousness with respect to independent Claims 1, 7, 12, 17, 21 and 27, and any claims dependent therefrom.

In view of the foregoing amendments and remarks, the cited references do not support the Examiner's rejection of Claims 27-31 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

V. Rejection of Claim 32 under 35 U.S.C. §103

The Examiner has rejected Claim 32 under 35 U.S.C. §103(a) as being obvious over Teng in view of the APA and Wu. As established above, each of the references Teng, the APA and Wu fails to teach or suggest the element that no structural interface exists between the first and second portions of the isolation region. As each of the references individually fails to teach or suggest such an element, the combination of those references must fail to teach or suggest such an element.

Therefore, the combination of Teng, the APA and Wu fails to teach or suggest each and every element of independent Claims 1, 7, 12, 17, 21 and 27, and as such, it fails to establish a *prima facie* case of obviousness with respect to independent Claims 1, 7, 12, 17, 21 and 27, and any claims dependent therefrom.

In view of the foregoing amendments and remarks, the cited references do not support the Examiner's rejection of Claim 32 under 35 U.S.C. §103(a). The Applicant therefore respectfully requests the Examiner withdraw the rejection.

VI. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-32.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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DOCKET NO. WYLIE 5

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

(1) Kindly rewrite Claim 1 as follows:

1. (Thrice Amended) A semiconductor device, comprising:

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(2) Kindly rewrite Claim 7 as follows:

7. (Thrice Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

a trench located adjacent a side of the channel region;

an isolation region located in the trench, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(3) Kindly rewrite Claim 12 as follows:

12. (Thrice Amended) A semiconductor device, comprising:

a channel region located in a semiconductor substrate;

an isolation region located adjacent the channel region, the isolation region being located within a trench formed in the semiconductor substrate and not extending under the channel region and including a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(4) Kindly rewrite Claim 17 as follows:

17. (Thrice Amended) A semiconductor device, comprising:

a first transistor located adjacent a second transistor, wherein both the first and second transistors are located over a semiconductor substrate;

an isolation region located between the first and second transistors and within a trench located within the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions; and

source/drain regions associated with each of the first and second transistors, each of the source/drain regions having a first portion located in the semiconductor substrate and a second portion located on the isolation region and in contact with the second post portion, but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(5) Kindly rewrite Claim 21 as follows:

21. (Thrice Amended) A method of manufacturing a semiconductor device, comprising:

providing a semiconductor substrate;

creating a gate above the semiconductor substrate;

forming an isolation region within a trench located in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;

forming a first portion of one of a source/drain region in the semiconductor substrate and a second portion of the one of the source/drain region on the isolation region and in contact with the

second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions.

(6) Kindly rewrite Claim 27 as follows:

27. (Thrice Amended) An integrated circuit, comprising:

semiconductor devices, including;

a semiconductor substrate;

a gate formed above the semiconductor substrate;

an isolation region located within a trench formed in the semiconductor substrate, wherein the isolation region includes a first portion and a second post portion located thereover, wherein no structural interface exists between the first and second portions;

a first portion of one of a source/drain region formed in the semiconductor substrate and a second portion of the one of the source/drain region formed on the isolation region and in contact with the second post portion but not in the semiconductor substrate, wherein an interface separates the first and second portions; and

interconnect structures contacting the semiconductor devices.